CLAIMS

What is claimed is:

Claim 1. A method of fabricating a semiconductor structure, comprising the steps of:

forming a $Si_{1-x}Ge_x$ layer on a substrate;

forming a plurality of channels in the $Si_{1-x}Ge_x$ layer and the substrate;

removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer to form a void in the substrate; and

filling the channels and the void with a dielectric material.

Claim 2. A method according to claim 1, wherein:

the substrate includes a first silicon layer, a second insulator layer and a third substrate layer;

the plurality of channels include at least a first channel and a second channel extending through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate; and

the void is formed in the first silicon layer of the substrate underneath the $Si_{1-x}Ge_x$ layer extending from at least the first channel to the second channel.

Claim 3. A method according to claim 1, wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of:

etching the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the substrate than for $Si_{1-x}Ge_x$;

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant from the group consisting of ammonia, tetramethyl ammonium hydroxide, nitric acid and hydrofluoric acid.

Claim 4. A method according to claim 3, wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface.

Claim 5. A method according to claim 4, wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface.

Claim 6. A method according to claim 2, wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer to form a void in the first silicon layer of the substrate from the first channel to the second channel produces a relaxed portion of the $Si_{1-x}Ge_x$ layer above the void.

Claim 7. A method according to claim 1, further comprising a step of annealing the $Si_{1-x}Ge_x$ layer after the void is formed in the first silicon layer.

Claim 8. A method according to claim 1, wherein the step of forming the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD);

limited reaction processing CVD (LRPCVD); and

molecular beam epitaxy (MBE).

Claim 9. A method according to claim 1, further comprising a step of forming a cap layer atop the $Si_{1-x}Ge_x$ layer.

Claim 10. A method according to claim 9, further comprising steps of:

removing the cap layer; and

forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer.

Claim 11. A method according to claim 1, further comprising a step of thickening the $Si_{1-x}Ge_x$ layer by forming a second $Si_{1-x}Ge_x$ layer on the first $Si_{1-x}Ge_x$ layer.

Claim 12. A method according to claim 1, further comprising a step of forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer.

Claim 13. A method according to claim 12, wherein the step of forming the strained semiconductor layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD)

limited reaction processing CVD (LRPCVD); and

molecular beam epitaxy (MBE).

Claim 14. A method according to claim 12, wherein the strained semiconductor layer is comprised of a semiconductor from the group consisting of Si and $Si_{1-y}C_y$.

Claim 15. A method according to claim 12, further comprising a step of forming a device on the semiconductor structure between the first and second channels as filled with dielectric material, and above the void as filled with dielectric material.

Claim 16. A method of fabricating a semiconductor structure, comprising steps of:

forming a $Si_{1-x}Ge_x$ layer on a silicon-on-insulator substrate having a first silicon layer, a second SiO_2 layer and a third substrate layer;

forming a first channel and a second channel, each channel extending through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate, the first channel and second channel being substantially parallel;

removing a portion of silicon layer under the $Si_{1-x}Ge_x$ layer to form a void in the first silicon layer of the substrate from the first channel to the second channel;

filling the first and second channels and the void with a dielectric material; and

forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer.

Claim 17. A method according to claim 16, further comprising a step of thermal annealing the $Si_{1-x}Ge_x$ layer after the void is formed in the first silicon layer and before the first and second channels and the void are filled with dielectric material.

Claim 18. A method according to claim 16, further comprising a step of planarization after filling the first and second channels and the void with a dielectric material.

Claim 19. A method according to claim 16, wherein the step of forming the $Si_{1-x}Ge_x$ layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD);

limited reaction processing CVD (LRPCVD); and

molecular beam epitaxy (MBE).

Claim 20. A method according to claim 16, wherein the step of forming the strained semiconductor layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD);

limited reaction processing CVD (LRPCVD); and

molecular beam epitaxy (MBE).

Claim 21. A method according to claim 16, further comprising a step of forming a cap layer atop the $Si_{1-x}Ge_x$ layer.

Claim 22. A Method according to claim 21, further comprising steps of:

removing the cap layer; and

forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer.

Claim 23. A method according to claim 16, wherein the step of forming a strained semiconductor layer includes a step from the group consisting of:

epitaxially growing a strained Si layer; and

epitaxially growing a strained $Si_{1-y}C_y$ layer.

Claim 24. A method according to claim 23, further comprising a step of thickening the $Si_{1-x}Ge_x$ layer by forming a second $Si_{1-x}Ge_x$ layer on the first $Si_{1-x}Ge_x$ layer.

Claim 25. An intermediate semiconductor structure comprising:

a substrate;

a relaxed $Si_{1-x}Ge_x$ layer on the substrate, the relaxed $Si_{1-x}Ge_x$ layer having at least one trench; and

at least one void between the relaxed $Si_{1-x}Ge_x$ layer and the substrate.

Claim 26. An intermediate semiconductor structure according to claim 25, wherein the substrate is comprised of a silicon-on-insulator wafer.

Claim 27. An intermediate semiconductor structure according to claim 25, wherein the thickness of the $Si_{1-x}Ge_x$ layer is less than a critical thickness for the $Si_{1-x}Ge_x$ layer.

Claim 28. An intermediate semiconductor structure according to claim 25, further comprising a strained semiconductor layer epitaxially grown on the relaxed $Si_{1-x}Ge_x$ layer.

Claim 29. An intermediate semiconductor structure according to claim 28, wherein the strained semiconductor layer is comprised of Si.

Claim 30. An intermediate semiconductor structure according to claim 28, wherein the strained semiconductor layer is comprised of $Si_{1-y}C_y$.